

Rejection of Claims Under 35 U.S.C. § 103(a)

Claims 1-25 and 49-61 are rejected as allegedly being unpatentable over Schueller (U.S. Patent No. 5,866,949) in view of Zenner et al. (U.S. Patent No. 6,246,010) and Welkowsky et al. (U.S. Patent No. 5,160,560) and the admitted prior art. Such a rejection is traversed as follows.

Claim 1 recites an integrated circuit package that comprises a silicon die that has a first thickness. A transition medium is disposed between the silicon die and a metallized polymer having a first side and a second side. The transition medium has a second thickness. The first thickness of the silicon die is less than the second thickness of the transition medium. None of the cited art, alone or in combination, describe or suggest a package that has a silicon die that is thinner than a transition medium.

In contrast, Schueller describes using a substantially rigid nonpolymer support structure to decouple the die from a substrate. The dies 52 illustrated in Figures 3A to 3D have a thickness that is greater than a thickness of the nonpolymer support structure 50. There is no description or suggestion of the desirability of using a die 52 that has a thickness that is thinner than the nonpolymer support structure.

While Zenner et al. does provide a semiconductor device ("die") 12 that has a thickness that is less than the thickness of Schueller's nonpolymer support structure, there is still no suggestion to a person of ordinary skill in the art to make the combination of the references. The mere fact that the references can be combined is insufficient to establish a *prima facie* case of obviousness. The prior art must suggest the desirability of the combination (MPEP § 2143.01).

The teachings of Zenner et al. appear to teach away from the proposed combination. In particular, Zenner et al. describes using a thin adhesive layer and a thin die so as to maintain a thin package thickness to allow for flexibility in the package. The thinness of the package allows the package to bend to relax the tensile and compressive stress remaining from the bonding process. (See Zenner et al. at col. 4, line 66 to col. 5, line 17). A person of ordinary skill in the art would not be motivated to combine a non-polymer support structure of Schueller with a thin silicon die of Zenner et al. since such a

combination increases the overall thickness of the package and would go directly against Zenner et al.'s teaching of providing a thin package so as to reduce the stress in the package.

For at least the above reasons, there is no suggestion to combine Schueller and Zenner et al. Therefore, claim 1 is allowable over Schueller and Zenner et al. Dependent claims 2-19 are allowable for at least the same reasons.

In regards to the combination of Schueller and Welkowsky et al., while Welkowsky et al. does provide a semiconductor wafer ("die") 12 having a thickness that is less than the thickness of Schueller's nonpolymer support structure, there is still no suggestion to a person of ordinary skill in the art to make the combination of the references. Similar to above, the mere fact that the references can be combined is insufficient to establish a *prima facie* case of obviousness. The prior art must suggest the desirability of the combination (MPEP § 2143.01).

There is also no description or suggestion of the desirability of combining Schueller and Welkowsky et al. Welkowsky et al. describes bonding a semiconductor wafer directly to a glass substrate using electrostatic bonding. Welkowsky et al. teaches away from using an adhesive to bond the wafer 12 to the substrate 16. In particular, Welkowsky et al. states:

"Since no adhesive is used, the wafer can be processed at extremely high temperatures. In an adhesive is used, processing at high temperatures could result in problems due to softening of the adhesive. Further, there is no layer of adhesive to affect the resulting optical quality." (Welkowsky et al. at col. 7, lines 51-56).

In contrast, Schueller illustrates multiple embodiments, all of which appear to use an adhesive. Because Welkowsky et al. teaches away from using an adhesive to bond the die to the substrate, a person of ordinary skill in the art would not be motivated to combine Schueller and Welkowsky et al. Consequently, independent claim 1 and dependent claims 2-19 are allowable over the combination of Schueller and Welkowsky et al.

Independent claim 20 provides an integrated circuit package comprising a metallized polymer layer defining a first thickness. A transition medium is coupled to the metallized polymer layer. A die is coupled to the transition medium. A mold cap encapsulates the transition medium and the die. The mold cap defines a second thickness, in which the first thickness and second thickness define a package thickness. The die is disposed near the middle of the package thickness. The cited art fails to describe or suggest the package of claim 20.

It is well settled that in order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a) that all of the elements of the claim must be described or suggested by the references. (MPEP § 2143). None of the cited references (Schueller, Zenner et al., or Welkowsky et al.) describe or suggest positioning the die near the middle of the package thickness. As is described in the specification on page 2, lines 6-17, the transition medium provides a stress relief buffer zone and moves the die toward the middle of the package thickness. Positioning the die near the middle of the package thickness maintains the die in a relatively motionless position during thermal cycling and reduces the warpage and curling of the package, thus extending the life of the electronic device. The cited art does not describe or suggest packages that provide such benefits. Consequently, independent claim 20 is allowable over the cited art. For at least the same reasons, dependent claims 21-24 are also allowable.

Independent claim 25 recites an integrated circuit package that comprises a tape carrier that defines a thickness. A first adhesive layer is disposed on the tape carrier. A first surface of a transition medium engages the first adhesive layer. A second adhesive layer is disposed on a second surface of the transition medium. A die is disposed on the second adhesive layer. A thickness of the die is less than the thickness of the transition medium. A mold cap encapsulates the first adhesive layer, transition medium, second adhesive layer, and the die. The thickness of the adhesive layers, transition medium and die is nearly equivalent to or the same as half of the package thickness. The transition medium and mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

For the same reasons as described above in relation to claims 1 and 20, claim 25 should also be allowable over the cited references. In particular, none of the references, alone or in combination, describe or suggest providing a die that has a thickness that is less than the thickness of the transition medium. Furthermore, none of the references describe or suggest having a thickness of the adhesive layers, transition medium and die to be nearly equivalent or the same as half of the package thickness. Therefore, claim 25 is allowable.

Independent claim 49 provides an integrated circuit package comprising an integrated circuit die having a front side, a back side, and a thickness between the front and back sides. A metallized polymer layer having first side and a second side is coupled to the die with a transition medium that has a thickness that is greater than the thickness of the die. Bonding pads are formed on the front side of the die and are electrically coupled to the metallized polymer layer. For at least the same reasons described above in relation to claim 1, independent claim 49 (and dependent claims 50-61) are allowable.

#### Added Claims

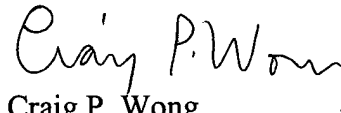
To more fully claim the novel aspects of the present invention, applicant has added claims 62-66. Independent claim 62 provides an integrated circuit package that comprises a substrate and a silicon die. A transition medium is positioned between the substrate and the silicon die. The transition medium comprises a thickness that is greater than the thickness of the silicon die. The cited art does not describe or suggest the package recited in claim 62.

CONCLUSION

In view of the foregoing, applicant believes all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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**APPENDIX A: VERSION WITH MARKINGS TO SHOW CHANGES MADE**

25. (Twice Amended) An integrated circuit package comprising:  
a tape carrier defining a thickness;  
a first adhesive layer disposed on the tape carrier, the first adhesive layer having a coefficient of thermal expansion and a thickness;  
a transition medium having a first surface and a second surface, wherein the first surface of the transition medium engages the first adhesive layer, the transition medium having a coefficient of thermal expansion and a thickness;  
a second adhesive layer disposed on the second surface of the transition medium, the second layer of adhesive having a coefficient of thermal expansion and a thickness;  
a die disposed on the second adhesive layer comprising a thickness that is less than the thickness of the transition medium; and  
a mold cap encapsulating the first adhesive layer, the transition medium, the second adhesive layer and the die, wherein the mold cap and tape carrier define a package thickness, wherein the thickness of the adhesive layers, transition medium and die is nearly equivalent to or the same as [the] half of the package thickness so as to reduce the stress on the die during thermal cycling, wherein the transition medium and the mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

62. (Added) An integrated circuit package comprising:  
a substrate;  
a silicon die comprising a thickness; and  
a transition medium positioned between the substrate and the silicon die,  
wherein the transition medium comprises a thickness that is greater than the thickness of  
the silicon die.

63. (Added) The integrated circuit package of claim 62 wherein the transition medium comprises a first adhesive layer positioned between the transition medium and the substrate, and a second adhesive layer positioned between the transition medium and the silicon die.

64. (Added) The integrated circuit package of claim 62 comprising a mold cap that encapsulates the silicon die and transition medium, wherein the mold cap and substrate define a package thickness, wherein the silicon die is positioned at approximately a middle of the package thickness.

65. (Added) The integrated circuit package of claim 62 wherein the transition medium comprises a mold compound material, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.

66. (Added) The integrated circuit package of claim 62 wherein the transition medium has a coefficient of thermal expansion between approximately  $7 \times 10^{-6}/^{\circ}\text{C}$  and  $17 \times 10^{-6}/^{\circ}\text{C}$ .

**APPENDIX B: CLEAN COPY OF ALL PENDING CLAIMS**

1. (As filed) An integrated circuit package comprising:  
a silicon die having a first thickness;  
a metallized polymer layer having a first side and a second side; and  
a transition medium disposed between the silicon die and the first side of the metallized polymer layer wherein the transition medium has a second thickness, and the first thickness of the silicon die is less than the second thickness.
2. (As filed) The integrated circuit package of claim 1 wherein the transition medium is nonconductive.
3. (As filed) The integrated circuit package of claim 1 comprising a plastic encapsulant which encapsulates the silicon die and the transition medium, the plastic encapsulant having a coefficient of thermal expansion between approximately  $7 \times 10^{-6}/^{\circ}\text{C}$  and  $15 \times 10^{-6}/^{\circ}\text{C}$ .
4. (As filed) The integrated circuit package of claim 1 wherein the transition medium comprises a mold compound material, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.
5. (As filed) The integrated circuit package of claim 1 wherein the transition medium has a coefficient of thermal expansion between approximately  $7 \times 10^{-6}/^{\circ}\text{C}$  and  $17 \times 10^{-6}/^{\circ}\text{C}$ .
6. (As filed) The integrated circuit package of claim 1 wherein the presence of the transition medium reduces stress and fracture damage to the silicon die.
7. (As filed) The integrated circuit package of claim 1 wherein a thickness of the metallized polymer layer and a thickness of the plastic encapsulant



define a package thickness, wherein the silicon die is disposed near the middle of the package thickness.

8. (As filed) The integrated circuit package of claim 7 wherein the package thickness is approximately 0.060 inches or less.

9. (As filed) The integrated circuit package of claim 5 wherein the silicon die thickness is less than approximately 6 mils.

10. (As filed) The integrated circuit package of claim 1 wherein the silicon die is coupled to the transition medium through an adhesive.

11. (As filed) The integrated circuit package of claim 1 wherein a coefficient of thermal expansion for the adhesive is approximately  $58 \times 10^{-6}/^{\circ}\text{C}$ .

12. (As filed) The integrated circuit package of claim 1 wherein the integrated circuit metallized polymer layer is a tape carrier having a dielectric layer and a conductive layer.

13. (As filed) The integrated circuit package of claim 12 comprising solder balls mounted to the second side of the metallized polymer layer, the solder balls electrically contacting an etched circuit in a conductive layer of the tape carrier.

14. (As filed) The integrated circuit package of claim 13 wherein the solder balls electrically connect the integrated circuit package to a printed circuit board.

15. (As filed) The integrated circuit package of claim 14 wherein the solder balls are arranged in a grid fashion underneath the position for the silicon die.

16. (As filed) The integrated circuit package of claim 1 wherein the cross sectional area of the silicon die is substantially less than or equal to the cross sectional area of the rigid transition medium.

17. (As filed) The integrated circuit package of claim 1 wherein the cross sectional area of the silicon die is larger than the cross sectional area of the transition medium.

18. (As filed) The integrated circuit package of claim 1 wherein the package is a BGA package.

19. (As filed) The integrated circuit package of claim 1 wherein a volume of the silicon die is less than the volume of the rigid transition medium.

20. (As filed) An integrated circuit package comprising:  
a metallized polymer layer defining a first thickness;  
a transition medium coupled to the metallized polymer layer;  
a die coupled to the transition medium; and  
a mold cap encapsulating the transition medium and the die, the mold cap defining a second thickness, wherein the first thickness and second thickness define a package thickness, wherein the die is disposed near the middle of the package thickness.

21. (As filed) The integrated circuit package of claim 20 wherein the mold cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the transition medium.

22. (As filed) The integrated circuit package of claim 20 wherein the die is mounted to the transition medium with a layer of adhesive.

23. (As filed) The integrated circuit package of claim 20 wherein the transition medium comprises a mold cap material, a second layer of adhesive, an elastomer, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.

24. (As filed) The integrated circuit package of claim 20 wherein the metallized polymer layer is a tape carrier.

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25. (Twice Amended) An integrated circuit package comprising:  
a tape carrier defining a thickness;  
a first adhesive layer disposed on the tape carrier, the first adhesive layer having a coefficient of thermal expansion and a thickness;  
a transition medium having a first surface and a second surface, wherein the first surface of the transition medium engages the first adhesive layer, the transition medium having a coefficient of thermal expansion and a thickness;  
a second adhesive layer disposed on the second surface of the transition medium, the second layer of adhesive having a coefficient of thermal expansion and a thickness;  
a die disposed on the second adhesive layer comprising a thickness that is less than the thickness of the transition medium; and  
a mold cap encapsulating the first adhesive layer, the transition medium, the second adhesive layer and the die, wherein the mold cap and tape carrier define a package thickness, wherein the thickness of the adhesive layers, transition medium and die is nearly equivalent to or the same as half of the package thickness so as to reduce the stress on the die during thermal cycling, wherein the transition medium and the mold cap have approximately the same coefficient of thermal expansion so as to reduce the thermal stress on the die during thermal cycling.

*Claims 26-48 previously canceled.*

49. (Previously amended) An integrated circuit package comprising:  
an integrated circuit die having a front side, a back side, and a first thickness between the front and back sides, wherein bonding pads are formed on the front side;  
a metallized polymer layer having a first side and a second side, wherein the bonding pads are electrically coupled to features of the metallized polymer layer; and

a transition medium, between the integrated circuit die and the metallized polymer layer, wherein the transition medium has a second thickness, greater than the first thickness.

50. (Previously added) The integrated circuit package of claim 49 wherein the front side of the integrated circuit die faces away from the metallized polymer layer.

51. (Previously added) The integrated circuit package of claim 49 wherein the integrated circuit die, metallized polymer layer, and transition medium are three parallel planes.

52. (Previously added) The integrated circuit package of claim 49 wherein the transition medium has a single, relatively uniform thickness.

53. (Previously added) The integrated circuit package of claim 49 wherein the integrated circuit package accommodates only a single integrated circuit die.

54. (Previously added) The integrated circuit package of claim 49 further comprising:

bonding wires to electrically couple the bonding pads to the features of the metallized polymer layer.

55. (Previously added) The integrated circuit package of claim 49 wherein the transition medium does not comprise metal.

56. (Previously added) The integrated circuit package of claim 49 wherein none of the bonding pads are electrically coupled to the transition medium.

57. (Previously added) The integrated circuit package of claim 49 wherein between the transition medium and the integrated circuit die is only an adhesive layer.

58. (Previously added) The integrated circuit package of claim 49 wherein the back side of the integrated circuit die faces toward the transition medium.

59. (Previously added) The integrated circuit package of claim 49 wherein the integrated circuit package is a ball grid array package.

60. (Previously added) The integrated circuit package of claim 49 wherein the transition medium has a coefficient of thermal expansion between approximately  $7 \times 10^{-6}/^{\circ}\text{C}$  and  $17 \times 10^{-6}/^{\circ}\text{C}$ .

61. (Previously added) The integrated circuit package of claim 49 further comprising:  
solder balls, below the metallized polymer layer and integrated circuit die, electrically coupled to the bonding pads.

62. (Added) An integrated circuit package comprising:  
a substrate;  
a silicon die comprising a thickness; and  
a transition medium positioned between the substrate and the silicon die, wherein the transition medium comprises a thickness that is greater than the thickness of the silicon die.

63. (Added) The integrated circuit package of claim 62 wherein the transition medium comprises a first adhesive layer positioned between the transition medium and the substrate, and a second adhesive layer positioned between the transition medium and the silicon die.

64. (Added) The integrated circuit package of claim 62 comprising a mold cap that encapsulates the silicon die and transition medium, wherein the mold cap and substrate define a package thickness, wherein the silicon die is positioned at approximately a middle of the package thickness.

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02 65. (Added) The integrated circuit package of claim 62 wherein the transition medium comprises a mold compound material, a BT resin compound, a FR-4 compound, or a FR-5 resin compound.

66. (Added) The integrated circuit package of claim 62 wherein the transition medium has a coefficient of thermal expansion between approximately  $7 \times 10^{-6}/^{\circ}\text{C}$  and  $17 \times 10^{-6}/^{\circ}\text{C}$ .

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